Review and perspective of tunnel currents for high-K dielectrics semiconductor

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Abstract

The paper reviews recent work in the area of high-*k* dielectrics for application as the gate oxide in advanced MOSFETs. The effect of dielectric constant and barrier height on the WKB modeled tunnel currents of MOS capacitors with effective oxide thickness of 2.0 nm is described. We first present the WKB numerical model used to determine the tunnelling currents. The results of this model indicate that alternative dielectrics with higher dielectric constants show lower tunnelling currents than SiOx at expected operating voltages. The results of SiOx/alternative dielectric stacks indicate currents which are asymmetric with electric field direction. All practical methods of preparation result in a thin interfacial layer generally of the form Si*Ox* or a mixed oxide between Si and the high-*k* so that the extraction of the dielectric constant is complicated and values must be qualified by error analysis. Furthermore, as the dielectric constant of an insulator increased, the effect of a thin layer of SiOx on the current Characteristics of the dielectric stack increases.

Introduction

The challenges around the search for a replacement for silicon dioxide as the gate dielectric in the ubiquitous CMOS technology are well known to the community. The unique and excellent intrinsic properties of SiO2 together with its compatibility with high temperature manufacturing process and the natural abundance of silicon, have underpinned the entire development of the silicon industry.

As MOSFET device dimensions continue to scale into the sub-0.1μm regime, the required SiO_2 gate dielectric thickness is projected to reduce below 2.5 nm and the voltage supply (V_{dd}) is projected to be from 0.8 to 1.8 V [1]. At these thicknesses and voltages, a large direct tunnel current density flows between the gate electrode and the silicon substrate [2]–[4]. This large direct tunnel current increases power consumption and reduces device performance making SiO_2 undesirable in this thickness regime [4]. Therefore, there has been much interest in finding a high-permitivity gate insulator with equivalent SiO_2 thickness and sufficient barrier height as a replacement for SiO_2 . However, since the barrier height tends to decrease with increasing dielectric constant [5], strong tradeoffs exist between various alternative dielectrics.

The well-known issue for the gate oxide then, is that it must become vanishingly thin to control adequately the electrostatics of the MOSFET channel and so win in the competition with the drain voltage encroachment ,to minimise undesirable short channel effects. In fact, the International Technology Roadmap for Semiconductors (ITRS) predicts equivalent oxide thicknesses of 1 nm in 2007, reducing to 0.35 nm for the 22 nm node [6].

In this work we provide a comparison of the WKB modelled tunneling currents of various representative dielectrics including: SiO_2 , Si_3N_4 , SiO_xN_y (silicon oxynitride), high dielectric constant (25–30) insulators, and insulators formed with a layer of SiO_2 and a high dielectric constant dielectric. The modelled tunnelling currents do not include the trap-assisted or Frenkel–Poole conduction mechanisms. Therefore, the results indicate the effect of changing the dielectric constant and barrier height of the insulator. Also, some authors have shown small trap densities for some of these dielectrics which would result in predominantly electron tunneling [7]–[9]. Overall, the goal of this study was to provide some initial first-order relationships for various dielectrics that may be used when considering development of any alternative dielectric for the gate insulator of MOS transistors.

Such oxide thickness reduction comes at a price as the quantum mechanical current leakage through the gate becomes prohibitively high and so therefore is the standby power dissipation in chips containing a billion individual transistors. The gate leakage must be reduced without

compromising the current drive (*ION*) of the transistor so materials with higher dielectric constant (k) are sought to allow a thicker oxide for the same gate capacitance, so mitigating the leakage problem. Silicon dioxide is a hard act to follow and any contender must satisfy stringent requirements. We can summarize the requirements [10] as relating to: thermodynamic stability in contact with Si; a high enough k to warrant the cost of R&D including a propensity to be scaled; band offsets for electrons and holes > 1 eV which translates to band gap energies (E_g) > 5 eV taking into account the inverse relationship between E_g and k; stability through a high temperature CMOS manufacturing process and finally, acceptable reliability and wear-outattributes.

2. k-dielectricphysics

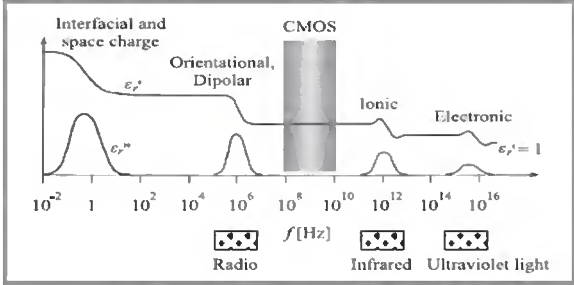

Fig . 1. The frequency dependence of the dielectric function [11].

Figure 1 presents a useful description of the frequency dependence of the dielectric function over a wide range of frequencies. In general, the "zero frequency" value of the dielectric constant can be seen to have two components: a "high – frequency" one, where the contribution of electronic polarization dominates and one related to the ionic contribution [12]. In the CMOS frequency window, we can see that electronic and ionic processes contribute to k and we consider that the permittivity is given by the relation:

$$\varepsilon_{ox} = \varepsilon_{\infty} + \varepsilon_{latt}$$

where ε_{ox} is equivalent to k.

The electronic component, which arises from simple polarization of the atoms, is the main component for SiO_2 and the simple relationship $n \sim \sqrt{\varepsilon_{\infty}}$ links the refractive index, readily measurable in ellipsometry , to the permittivity, giving $\varepsilon_{ox} \sim \varepsilon_{\infty}$. The essence of increasing k then is to choose materials that can contribute a large lattice component. Table 1 shows some values of these parameters for different crystalline forms of hafnia. We can see that ε_{latt} can vary from about 2 to over 25 depending on

TABLE I

Crystalline phase	ε_{∞}	ε_{latt}	$\varepsilon_{ox}(k)$
c-HfO_2	5.37	20.80	26.17
t-HfO_2: parallel	5.13	14.87	20.00
t-HfO_2: perpendicular	5.39	27.42	32.81
m-HfO_2: yy	–	10.75	10.75
m-HfO_2: xx	–	11.70	11.70
m-HfO_2: zz	–	7.53	7.53
m-HfO_2: xz	–	1.82	1.82

The electronic (ε_{∞}) and lattice (ε_{latt}) permittivity components for different crystalline forms of hafnia [5] the crystalline form. Without going into details of the crystallography, we can simply make the point that the permittivity can vary over a wide range depending on the form of the material and

hence the method used to prepare it. Furthermore, amorphous forms are preferred for processing in any event. The variability of k with the structure of various metallic oxides is pointed out from another perspective in [13], by consideration of the Clausius-Mossotti (C-M) theory which links the k to the polarizability α, and the volume of the unit cell, V_m as described in Eq. (2):

$$\varepsilon_r = \frac{\left(1+\frac{2}{3}4\pi\frac{\alpha}{V_m}\right)}{1-\frac{1}{3}4\pi\frac{\alpha}{V_m}} \qquad (2)$$

In essence, larger atoms yield more polarization and hence higher k values. The C-M equation reveals that k raises steeply as the ratio □/ V_m increases demonstrating the strong connection with the structure and nature of the material.

3. TUNNELING MODEL

The following is a description of the model used to calculate the tunneling currents of n^+p capacitors in accumulation for a Semiconductor Insulator Semiconductor (SIS) system based on a simple numerical calculation of the WKB transmission coefficient assuming equilibrium in the substrate and gate and no trap-assisted conduction. The first part of the numerical calculations was to determine the SIS parameters with an insulator whose dielectric constant and band gap varies as a function of distance. The insulator
Capacitance (C_i) was calculated using

$$C_i = \left[\int_0^{t_{ox}} \frac{dx}{\varepsilon(x)}\right]^{-1} \qquad (3)$$

Where t_{ox} is the physical oxide thickness and is the dielectric constant as a function of distance in the insulator. The flat band voltage (V_{fb}) was calculated from the difference between the gate and substrate Fermi potentials which were determined using full Fermi–Dirac statistics [14], [15]. The gate and substrate surface potentials (ψ_{gate}, ψ_{sub}) were numerically solved from the potential and charge balance equations, (4), (11)

$$V_g = \psi_{gate} + \psi_{sub} + V_{fb} - \frac{Q_{sub}(\psi_{sub})}{C_i} \qquad (4)$$

$$Q_{sub}(\psi_{sub}) + Q_{gate}(\psi_{gate}) = 0 \qquad (5)$$

Where Q_{sub} and Q_{gate} are the substrate and gate semiconductor charge found using full Fermi–Dirac statistics[14,15] and V_g is the gate voltage. The oxide charge was assumed to be zero (Q_{ox}). The potential distribution inside the insulator [$V_i(x)$], total insulator potential drop (V_{ins}) and average insulator electric field $\left(F_{ins} = V_{ins}/t_{ox}\right)$ were then found by solving the Poisson equation. Finally, the insulator conduction band distribution [$E_{ci}(x)$] was determined using

$$E_{ci}(x) - E_{cg} = \phi_g(x) - qV_i(x) \qquad (6)$$

Where E_{cg} is the calculated polysilicon gate conduction band energy at the gate/insulator interface and ϕ_g (x) is the electron affinity difference between the dielectric and polysilicon (i.e., insulator conduction band distribution at flatband). The effects of image forces were ignored. The second part of the numerical analysis was the calculation of the tunneling current based on these SIS parameters and insulator conduction band. It was assumed that the tunnelling current is due only to conduction band electron which is a good assumption for an n^+p system biased in accumulation [16]. The tunnelling current density from the gate (J_g) was calculated assuming an independent electron approximation and an elastic tunneling process[17] using the following formula [2], [15]

$$J_g = \frac{4\pi q m_t}{h^3}\int_0^{E_{fg}} dE \int_0^{E} T_t(E, E_t)dE_t \qquad (7)$$

Where E_t is the transversal energy, m_t is the transversal effective mass (~ 0.19 m_e), E_{fg} is the gate Fermi level at the gate/insulator (injecting) interface, E is the total energy of the tunneling electron measured from E_{cg}, T_t, is the tunnelling transmission probability, q is the electronic charge, and ħ is Planck's constant. Assuming a one-band parabolic dispersion relation for the insulator conduction band, T_t can be calculated using the WKB approximation as[2,18].

$$T_t(E,E_t) = e^{\left(-\frac{2}{\hbar}\int\sqrt{2m_tE_t-2M_i[E-E_{ci}(x)]}\right)dx} \tag{8}$$

where is the insulator effective mass which is assumed constant. The integration in (8) is over all real values of the argument since we are assuming an elastic tunnelling process. We have also assumed as in [15] that a single transmission probability T_t(E, Et) = $T_t(E_{cg}, E_{cg})$ applies to all transitions in calculating the tunneling current. This approximation reduces (7) to

$$J_g = \frac{4\pi q m_t}{h^3}\frac{(E_{fg}-E_{cg})^2}{2}T_t(E_{cg},E_{cg}) \tag{9}$$

The goal in using the above numerical model is to provide an indication of the trends expected when changing the dielectric constant and barrier height of the insulators. These tunnelling calculations have a number of approximations that must be considered. Quantum-mechanical quantization effects in the semiconductor were not included. However, these quantum mechanical effects have been shown to not strongly effect calculated, is tunneling currents due to compensating effects if the calculations are performed relative to insulator potential [3]. However, for devices with thicknesses in this regime, these quantization effects must be considered when calculating surface potentials, oxide potentials, etc., as a function of gate voltage. Another issue is in the use of the WKB solution for these structures. Although the WKB solution has been shown to provide a reasonable fit to experimental data by fitting the effective mass and barrier height [2], [15], [16], the physical basis for this model for ultrathin dielectrics has been debated [3]. Furthermore, we have used a constant effective mass for all energies, thicknesses and dielectrics which may not be appropriate. There is a lack of reliable effective mass values for various dielectrics. The effective masses of the alternative dielectrics may be different and could change the magnitude of the differences in tunneling current. However, these WKB numerical calculations will provide a first order indication of the impact of dielectric constant and barrier height on tunneling currents to be used to indicate general trends expected for future dielectrics.

$$T_{fn}(E,E_t) = e^{-\frac{4(2\pi)}{3}\frac{\sqrt{2m_i}}{qh}\frac{\left(\phi g+E_{fg}-E+\frac{m_t}{m_i}E_t\right)^{3/2}}{F_{ins}}} \tag{10}$$

$$T_d(E,E_t) = e^{-\frac{4(2\pi)}{3}\frac{\sqrt{2m_i}}{qh}\frac{\left(\phi g+E_{fg}-E+\frac{m_t}{m_i}E_t\right)^{3/2}-\left(\phi g+E_{fg}-E+\frac{m_t}{m_i}E_t\right)^{3/2}+qV_{ins}}{F_{ins}}} \tag{11}$$

To check the accuracy of our numerical calculations, the current density for a SiO_2 layer with thickness of 2.0–4.0 nm was calculated using our numerical model and compared with the current density calculated using a full numerical integration of (5) with analytical expressions for the transmission coefficients. This was done to ensure that our numerical solution correctly fit other similar WKB formulations. The transmission coefficients previously determined for direct and Fowler–Nordheim tunneling (T_{fn}, T_d) into SiO_2 with a constant barrier height (ϕ_g) and constant dielectric constant are shown in (10) and (11) [2]. Table II gives the parameters assumed for the gate electrode and Si substrate and Table II contains the parameters assumed for the SiO_2 insulator. We have fit this numerical model to experimental data for SiO_2 down to 2.0 nm using an effective mass of m_i = 0.32m_e. A constant effective mass of m_i = 0.32 was assumed for these calculations [2]. The results shown in Fig. 2 indicate good agreement between the models suggesting that our numerical formulation is in agreement with other WKB calculations. The tunneling model described in the previous section was used to compare the tunneling currents of a

variety of insulators termed: SiO_2, Si_3N_4, $SiO_x N_y$, D1, and D2. Dielectric/SiO_2 stacked structures were also examined.

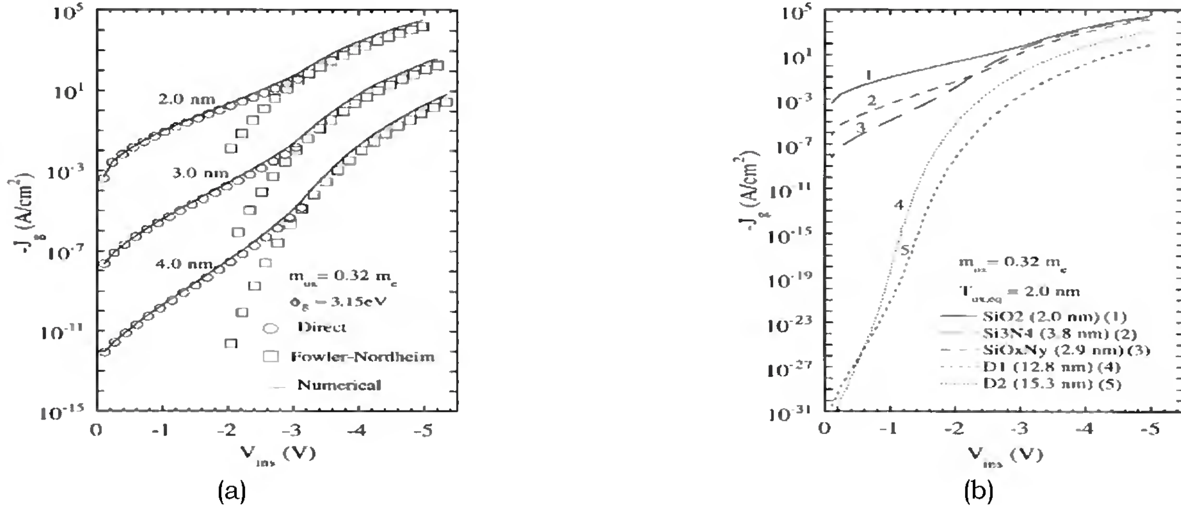

Fig. 2. (a) Comparison of numerical WKB model of calculating tunnelling current for SiO_2 to a full numerical integration of (5) and previously determined Fowler–Nordheim tunneling into SiO_2 [2].

(b) Tunneling current versus insulator potential for n^+p capacitors with various dielectrics having equivalent oxide thickness of 2.0 nm.

TABLE II: Gate Electrode and si Substrate Semiconductor parameters used in calculating the Tunneling currents.

	Gate Electrode	*Si Substrate*
Dielectric Constant (ε)	$11.8\varepsilon_o$	$11.8\varepsilon_o$
Doping (N_d, N_a)	$1.00 \cdot 10^{20}$ cm^{-3}	$2.00 \cdot 10^{17}$ cm^{-3}
Dopant Ionization Energy (E_c–E_d, E_c–E_a)	0.045 eV	1.075 eV
Energy Gap (E_g)	1.12 eV	1.12 eV
Effective Density of States in Conduction Band (N_c)	$2.80 \cdot 10^{19}$ cm^{-3}	$2.80 \cdot 10^{19}$ cm^{-3}
Effective Density of States in Valence Band (N_v)	$1.04 \cdot 10^{19}$ cm^{-3}	$1.04 \cdot 10^{19}$ cm^{-3}
Intrinsic Carrier Concentration (n_i)	$1.45 \cdot 10^{10}$ cm^{-3}	$1.45 \cdot 10^{10}$ cm^{-3}

TABLE III Insulators dielectric constant and barrier height used in calculating the Tunneling currents. The Barrier Height is defined as the Conduction Band Discontinuity between the Insulator and Silicon

	Dielectric Constant (ε)	*Barrier Height*
SiO_2 [9]	$3.9\varepsilon_o$	3.15 eV
Si_3N_4 [9]	$7.5\varepsilon_o$	2.10 eV
SiO_xN_y	$5.7\varepsilon_o$	2.60 eV
D1	$25.0\varepsilon_o$	1.30 eV
D2	$30.0\varepsilon_o$	1.00 eV

Table III indicates the dielectric constant and barrier height used for each of the insulators. The oxynitride film (SiO_2N) has an assumed dielectric constant and barrier height halfway between the values for Si_3N_4 and SiO_2 [14]. The values chosen for D1 and D2 are representative of several higher dielectric constant (high-K) alternative insulators (e.g., TiO_2, Ta_2O_2) [5],[7]–[8], [19]. The tunnelling currents from the gate were calculated assuming and the tunnelling currents from the gate were calculated assuming an n^+p capacitor with the parameters given in Table II.

Fig. 2(b) shows the tunnelling currents calculated for each of the dielectrics as a function of total insulator potential drop. The results indicate that for very low voltages, the insulators with the highest dielectric constant show the lowest tunnelling currents. The currents for D1 and D2 are observed to cross at $V_{ins} > \phi_g$. This cross-over can be qualitatively explained by considering that the current (9) is proportional to the transmission coefficient (8). The transmission coefficient is inversely and exponentially dependent on an integration of the square root of the insulator conduction band in which the electron travels under (which we will call barrier area). Therefore, the cross-over occurs when the increase of barrier area due to the tunneling distance of D2 is compensated for by the increase in barrier area due to the barrier height of D1. A large increase of current for each of the insulators is observed for $V_{ins} > \phi_g$ because the tunneling electrons begin to tunnel through less of a distance and enter the insulator conduction band (Fowler–Nordehim tunnelling). The results suggest that to reduce the expected tunnel current, it is more beneficial to have a high-k dielectric with ϕ_g slightly higher than the expected supply voltage ($V_{dd} \approx 1$ V) for T_{ox}=2.0 nm, than to have an insulator with slightly higher dielectric constant but lower ϕ_g. It is also observed that Si_3N_4 and SiO_xN_y show modest improvements over SiO_2. However, these insulators with do not have the high dielectric constant needed to further reduce the current.
The results of Fig. 2(b) indicate that replacement of SiO_2 with alternative dielectric results in a reduction of tunnel current which is most significant at lower voltage. However, instead of using only and alternative dielectric, many researchers have used SiO_2 /alternative dielectric stacks [7], [20]–[22]. The reasons for this include controlling interface state density and modifying barrier properties. Also, the SiO_2 in these stacked structures can be present as a native oxide at the Si interface [23]. Fig.3(a) and 3(b) show the calculated tunneling currents for D1/SiO_2 and Si_3N_4 /SiO_2 stacked structures, respectively. The insulator which is listed first is the dielectric which the electron first tunnels through. The change in the order of the insulator stack is equivalent to changing the electric field direction on this stack.

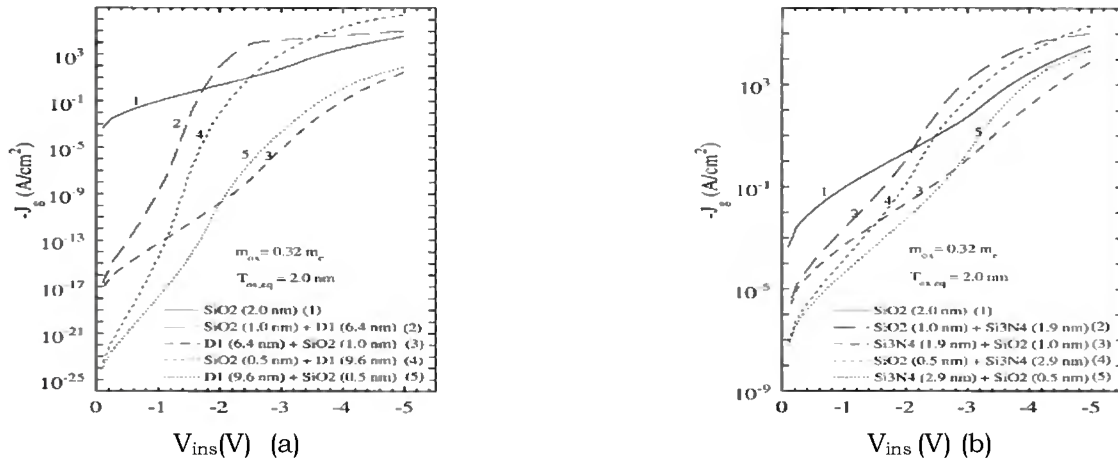

Fig 3. (a) Tunnelling current versus insulator potential for n^+p capacitors with D1/SiO_2 stacked dielectrics having equivalent oxide thickness of 2.0 nm. (b) Tunnelling current versus insulator potential for n^+p capacitors with Si_3N_4/SiO_2 stacked dielectrics having equivalent oxide thickness of 2.0 nm.

It is observed that the tunnelling currents change dramatically depending on which insulator the electron first tunnels through. Specifically, the tunnel current is much higher if the electron first tunnels through the higher barrier height material (SiO_2). This can be best understood by considering the insulator conduction band diagrams given in Fig. 4 for the SiO_2 (1.0 nm)/D1 (6.4 nm) stacks for V_{ins}= -2.38. It is observed that at this voltage (and above), an electron which first tunnels through the SiO_2 , no longer tunnels through any of the D1 barrier so that the tunnelling is determined only by the 1.0 nm SiO_2 barrier. However, an electron which first tunnels through the D1 barrier, will also tunnel through the SiO_2 barrier for these voltage ranges.

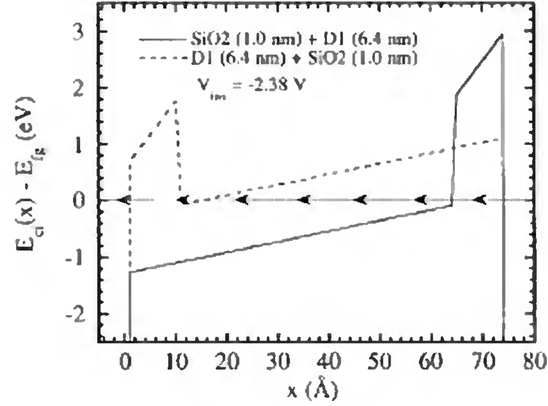

Fig 4. Insulator conduction band distribution referenced to the gate Fermi level for SiO_2 (1.0 nm)/D1 (6.4 nm) stacked dielectrics at an insulator potential of -2.38 V.

The approximately corresponds to the condition when the SiO_2 layer drops a voltage equivalent to the barrier height of the second layer. Fig. 5 shows the insulator conduction band for SiO_2 (0.5 nm)/D1 (9.6 nm) stacks for the same voltage (V_{ins}=-2.38 V). Comparison of Fig. 3(a) and 3(b) indicate that for this insulator potential, an electron will tunnel through a larger portion of the barrier for stacks with thinner SiO_2 regions. When the bias is increased further, an electron which first tunnels through the 0.5 nm SiO_2 barrier will no longer tunnel through the D1 barrier so that the tunnelling is determined only by the 0.5 nm SiO_2 barrier. Therefore, for very high biases, the tunnelling current for the SiO (0.5nm) + D1 (9.6 nm) stack will be greater than the tunnelling current for the SiO_2 (1.0 nm) +D1 (6.4 nm) since the tunnelling distance is shorter.

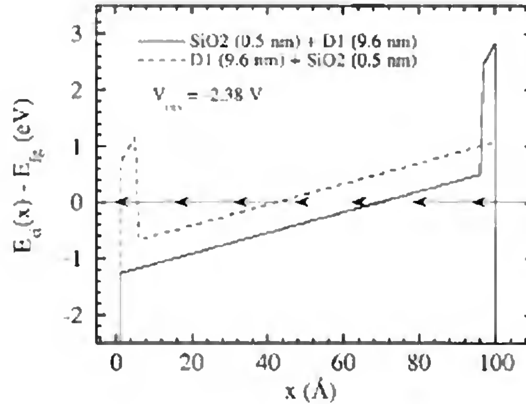

Fig 5. Insulator conduction band distribution referenced to the gate Fermi level for SiO_2 (0.5 nm)/D1 (9.6 nm) stacked dielectrics at an insulator potential of -2.38 V.

Comparing Fig. 3 and 4 shows that stacked insulators using Si_3N_4 result in smaller current changes than in using D1. This is simply because the current for biases when the electron is tunnelling through the entire barrier is closer to the current for biases when the electron is tunnelling only through the SiO_2. Furthermore, the barrier heights and dielectric constants of the Si_3N_4 and SiO_2 insulators are much closer than D1 and SiO_2 so that the total barrier for the electron is less affected for the Si_3N_4/SiO_2 stacked structures. This result indicates that a thin layer of SiO_2 with Alt1 results in a drastic difference in current as compared to Si_3N_4.

4. Methodologies to measure K-Dielectric

The simplest, most convenient and appropriate way to measure *k* is from a C-V plot although care is required to ensure that a genuine response is obtained which usually means adjusting the data for a variety of frequency dependent parasitic phenomena such as series resistance [24], leakage current [25] and lossy interfacial capacitance [26]. Furthermore, in the case of ultra-thin gate dielectrics, the accumulation capacitance does not readily saturate to the oxide capacitance *Cox*,

because the oxide capacitance is large compared to that of the space charge in accumulation and also due to the quantization of energy levels in the accumulation layer. The difference between the measured accumulation capacitance and the true oxide capacitance must be taken into account in the extraction of capacitance equivalent thickness (CET) and the effective dielectric constant. The Maserjian technique [27] provides a simple method to extract the oxide capacitance from a C-V plot under accumulation conditions. Computer code is available to account for accumulation layer related quantum mechanical effects and oxide leakage [28]. Having obtained a genuine accumulation and hence oxide capacitance, *Cox* (considered here per unit area) and if no transition layer (SiO_x) is present, the permittivity can simply be obtained from the relation that k = *Cox tox*, where *tox* has been measured from ellipsometry . In practice, and usually intentionally, a so-called transitional layer (TL) is present between the substrate and the high-k layer and a two-capacitor model (with perfect, planar interfaces, i.e., no roughness) can be used to analyse the MOS structure which may be written:

$$\frac{EOT}{\varepsilon_{SiO_2}} = \frac{t_{TL}}{\varepsilon_{TL}} + \frac{t_{hi-K}}{K} \qquad (12)$$

Where, we extend the definition of equivalent oxide thickness (EOT) to incorporate the TL. The electronic properties of TL are dependent on the nature of its formation and it can be designated SiO_x in general where often x=2 is used and the permittivity of 3.9 is then considered. However, it is important to note that x-values greater or less than 2 can arise therefore affecting the permittivity value; for instance, x>2 for oxides that are heavily strained, and x<2 for "unintentional" oxides that grow after an HF dip treatment. It is important therefore to understand the nature of the oxide and if possible measure its electrical and optical properties independently. We have illustrated the importance of this issue in a recent publication [29] and the main points are summarized here. We considered four samples of varying Hf stoichiometry with TLs produced by rapid thermal oxidation (RTO) and so-called chemical oxidation associated with $SC1/SC_2$ cleaning procedures. The chemical nature of the TL plays a major role in the growth dynamics of the HfO_2 layer; it has been shown that the use of chemical oxides, which are characterized by higher OH concentration, results in almost linear growth, while obtaining a two-dimensional uniform coverage with HfO_2 [30]. The thickness of the TL was measured in situ prior to the deposition by angle resolved X-ray photoelectron spectroscopy (ARXPS), that of the hafnia layer by spectro-ellipsometry and the Hf content by Rutherford backscattering spectrometry (RBS). The SE measurements were performed in the 184–1700 nm spectral range, at three various angles of incidence (65°, 70°, and 75°) for an increased sensitivity. A simple model was used for establishing the thickness of the HfO_2 film. The model incorporated a Si substrate and a TL for which the optical properties were established on a control sample together with a Cauchy layer for describing the hafnia layer. The thickness of the hafnia layer was extracted in the spectral region where the HfO_2 layer was transparent.

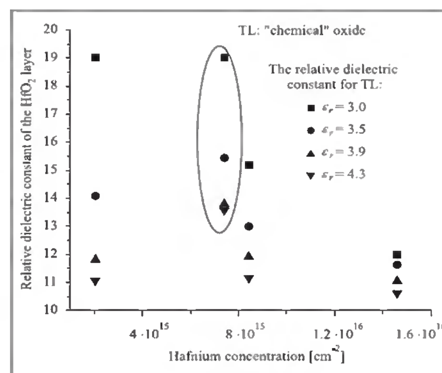

Fig 6. Relative dielectric constant of the HfO_2 layer versus Hf content calculated for different values of relative permittivity of transitional layer [29].

The maximum capacitance was measured and the model of [29] used to extract k using four values for ε_{TL}, in the 3-4.3 range. This choice of values for the ε_{TL} has been observed in TL's in our experience and also reported in the literature. Figure 5 shows the results of the extraction and it is striking that the spread of the k-values is relatively large (10.6–19). When increasing the [Hf] concentration in the layers, the spread of results is reduced significantly from factors of ~7 to ~1. Furthermore, for the same thickness of TL and nearly the same concentration of Hf, the samples with the chemical oxide TL have significantly higher relative dielectric constant: (14–19), as compared to 12–15. These results demonstrate the sensitivity of the extraction technique to the TL characteristics. Clearly for low Hf density, there is doubt that the model of Eq. (12) is valid and suggests a non-uniform or mixed TL and possible poor morphology of the hafnia layer. This point was pursued in the study of [31] where the effects of pre-treatment were investigated.

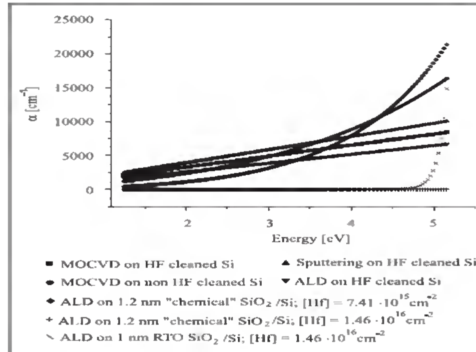

Fig 7. The absorption coefficient α versus energy for hafnia layers prepared by different techniques [31].

Figure 8 shows the absorption coefficient (α) extracted from the imaginary part of the complex permittivity, measured with SE. The best result (lowest α) is obtained with atomic layer deposition (ALD) on chemical oxide TL with ALD on RTO exhibiting a sharp increase in absorption at an energy E ~ 4.7 eV. There is some evidence that such an energy level is associated with the oxygen vacancy in hafnia films [32]. The worst case is for a film on chemical oxide with sub-stoichiometric Hf. Other samples in the study incorporated HF surface preparation and inferior properties are apparent for both ALD and metal organic chemical vapour deposition (MOCVD) hafnia deposition. We can summarise this section by reinforcing the importance of taking careful consideration of the TL when extracting k from C-V data and would advocate the use of error bars and a clear description of methodology when quoting experimental values.

The relative permittivity value using the Clausius-Mossotti equation (see relation (2)). Figure 7a shows the relative permittivity values versus the mean atomic number of some well-known and potentially suitable metal oxides, after Engstrom *et al.* [13]. In the same work, Pauling electro negativities were considered to allow prediction of the conduction band offsets for the oxides for which values were experimentally unknown, allowing predictions of conduction band offsets versus relative permittivity, as shown in Fig.9.

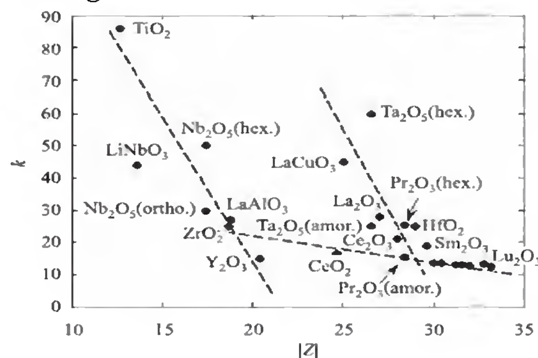

Fig 8. Experimental relative permittivity for some experimental gate dielectrics plotted against their mean atomic number [13].

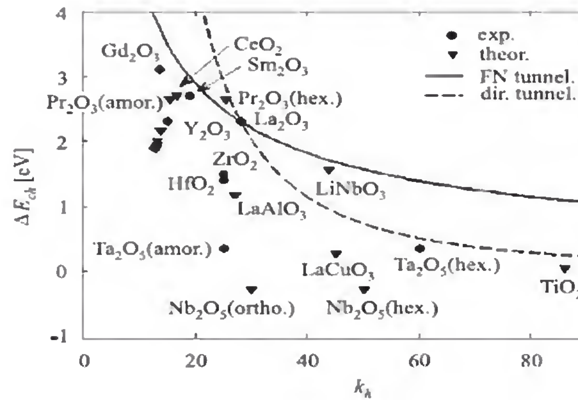

Fig 9. Conduction band offset versus the relative permittivity for experimental high-k dielectrics [13].

SUMMARY

The most pessimistic scenario, which was that any materials with relative permittivity lower than that of lanthanum would suffer from direct tunnelling and above this Fowler-Nordheim tunnelling. The tunneling currents for insulators with an effective oxide thickness of 2.0 nm were modeled using a numerical calculation of the WKB tunneling current. Model was shown to agree with previously determined analytical WKB formulations of tunneling current for SiO_2 . The numerical tunneling model was first applied to alternative dielectrics having different barrier heights and dielectric constants. The results indicated that alternative dielectrics with higher dielectric constants resulted in lower currents at low biases. It was predicted that only a few materials would be able to meet the requirements However, it was concluded that it is more beneficial to have a high- dielectric with barrier height slightly higher than the expected supply voltage, than to have an insulator with slightly higher dielectric constant.

The simplest way to measure k is from a C-V plot although care is required to ensure that a genuine response is obtained which usually means adjusting the data for a variety of frequency dependent parasitic phenomena. The above calculations show that if an alternative high dielectric constant material is to replace SiO_2 , then it will be necessary to find one with a barrier height greater than the applied voltage and one that can be fabricated with a few atomic layers (or less) of SiO_2 at the interface. This may prove to be a difficult challenge for future IC manufacturing.

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